## REMARKS

In accordance with the foregoing, claims 1-21, 24, 25, 27-30, 33, 34, 36-39 and 41 are been amended. No new matter is presented in any of the foregoing and, accordingly, approval and entry of the amended claims are respectfully requested.

Claims 1-41 are pending and under consideration.

### ENTRY OF AMENDMENT UNDER 37 CFR §1.116

Applicant requests entry of this Rule 116 Response because it is believed that the amendment of claims 1-21, 24, 25, 27-30, 33, 34, 36-39 and 41 puts this application into condition for allowance and should not entail any further search by the Examiner since no new features are being added or no new issues are being raised.

Claims 1, 12, 13, 14, and 41 are amended to respectively recite a method, an apparatus, and a computer-readable recording medium, using claim 1 as an example, including "a request for hardware resource data relating to a hardware resource . . . to a resource manager which manages said hardware resource data; allocating a resource in which said resource manager allocates said hardware resource data . . . while dynamically allocating hardware resource data relating to necessary hardware resources." Respective dependent claims are amended accordingly.

### ITEMS 2-3: OBJECTION TO CLAIMS 6, 17, AND 41

In items 2-3 of the Office Action, the Examiner objects to claims 6, 17, and 41 because of informalities. Claims 6, 17, and 41, are amended herein as suggested by the Examiner. Withdrawal of the objection is requested.

### ITEMS 6-18: REJECTION OF CLAIMS 1-41 UNDER 35 U.S.C. §103(A)

In items 6-18 of the Office Action, the Examiner rejects claims 1-41 under 35 U.S.C. §103(a) as being unpatentable over Chen (U.S.P. 6,466,898) in view of combinations of Dearth et al. (U.S. P. 6,345,242), Dearth et al. (U.S. Patent 5,812,824), Hollander (U.S.P. 6,347,388), Kinzelman et al. (U.S. P. 5,594,741), De Yong et al. (U.S.P. 5,355,435), Thekkath et al. (U.S.P. 6,490,642), Markov (U.S. P. 6,314,552), Kasuya (U.S.P. 6,077,304) Furuichi (U.S.P. 5,437,037) and Levy et al. (U.S.P. 6,092,175).

The rejections are traversed.

#### Features Not Taught by Cited Art

Independent claims 1, 12, 13, 14, and 41 (all as amended) respectively recite a method of simulating an operation of a logical unit, an apparatus, a computer-readable recording

medium, including, using claim 1 as an example, "requesting a resource in which a thread manager, which controls threads each forming an execution unit of a program, makes a request a request for hardware resource data relating to a hardware resource . . . to a resource manager which manages said hardware resource data; allocating a resource in which said resource manager allocates said hardware resource data . . . while dynamically allocating hardware resource data relating to necessary hardware resources (emphasis added)."

None of the cited art, alone or in combination, teaches such a request for hardware resource data and dynamically allocating hardware resource data. In item 19.1 of the Office Action, the Examiner contends that Levy et al. teaches:

> dynamically allocating necessary hardware resources to the thread by said resource manager every time the generated thread is executed.

That is, Levy does not teach allocating of data, as recited in each of the independent claims.

Rather, Levy merely discusses that a renaming of actual registers, that is real hardware resources, and not data, are dynamically allocatable and assignable to different threads at different times and are thus shared between the threads. That is, Levy does not teach a technique of a simulation of a logical unit.

Accordingly, none of the cited art, alone or in an *arguendo* combination teaches a simulation using hardware resource data relating to necessary hardware resources as recited in each of the independent claims.

**No Motivation To Combine The Art In A Manner As Suggested By The Examiner**

In item 6.1 the Examiner contends it would have been obvious to modify the method of Chen with the method of Levy:

> because that would support out-of-order execution of instructions . . . thus improving the performance of multithreaded processor

(Action at page 7).

Applicants submit there is no motivation or reasonable chance of success to modify the HDL (hardware restricted code) of Cohen with Levy.

Levy discusses (see, for example, col. 3 starting at line 10) "renaming registers are dynamically allocatable and assignable to different threads at different times and are thus shared between the threads." However, Cohen, for example, (col. 17, lines 40-50) discusses:

> (t)hus, to ensure the multithreaded simulator provided by the invention capable of minimizing these overheads, a variety of following methods are employed . . . keep the threads "alive" and be bound to hardware CPU as long as possible.

(Emphasis added)

That is, there is no motivation to modify the HDL code of Cohen with Levy as the Examiner contends.

**Summary**

Since features recited by independent claims 1, 12, 13, 14, and 41 (all as amended), and respective dependent claims are not taught by the cited art, alone or in combination, and there is no reasonable chance of success to combine the art, in a manner as the Examiner suggests, *prima facie* obviousness is not established and the rejection should be withdrawn and claims 1-41 allowed.

**CONCLUSION**

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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